ECE 478 HOMEWORK III

1-) What is pipelining? Advantages and disadvantages? Find a VHDL code example about pipelining. Compare RTL schematics and simulation results the cases of pipelined and without pipelined versions of the same operation. Add your codes also.

2-) Design a PWM signal generator. Design should have two inputs as clock and duty cycle, one output as PWM output. Add your design and simulation codes to your solution with your simulation results.

Deadline: 01.06.2018