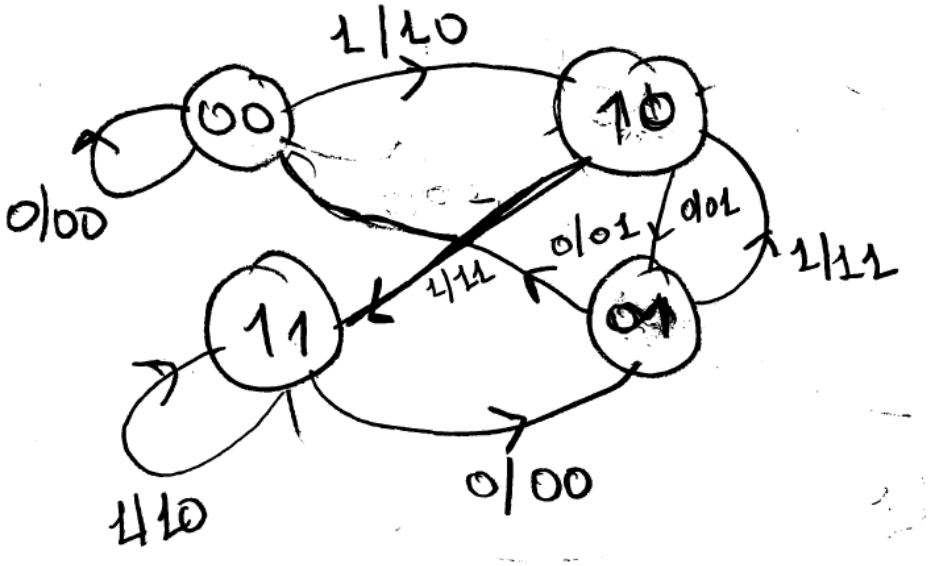
ECE 478 HOMEWORK II

1-) Implement below state diagram in VHDL. Simulate your program. Set input sequence as "011001010". Include your design codes, simulation codes and simulation results in your solution.



2-) Implement an 3 –bit binary up/down counter. If input equals to '0' then counter counts upward. When input equals to '1' the counter counts downward. Draw its state diagram. Include your design codes, simulation codes and simulation results in your solution.

Deadline: 15.03.2018