ECE 478 Lab-8

Implement the FIFO logic whose operation is explained in the Figure below in VHDL.

FIFO Interface

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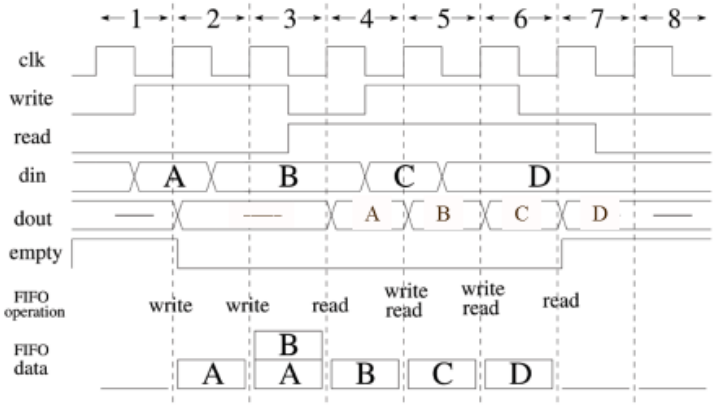
Operation of the "Standard" FIFO



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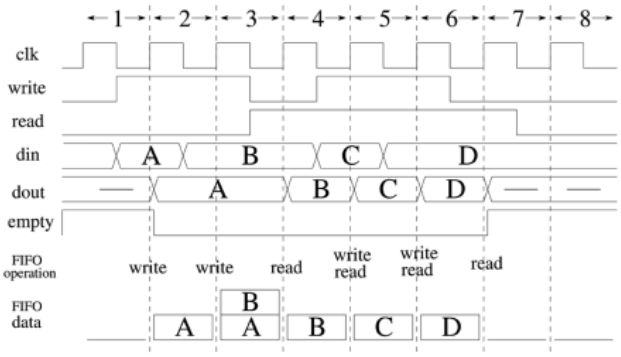
Operation of the First-Word Fall-Through FIFO



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